HiPer Consortium workshop

The workshop takes place on 1st of June 2016 at the Faculty of Engineering building (Bar-Ilan University), starting at 09:00

09:00 - 09:30 Registration and Breakfast

Opening: Description of the Consortium, its work and achievements

- Mr. Shay Adar, CEVA
- Mr. Ilan Peled, MAGNET Program
- Mr. Rafi Retter, HiPer Consortium

Keynote:

10:00 - 10:45

Prof. Luca Benini, ETH Zurich and University of Bologna
"Sub-Picowatt per Operation scalable computing - Why, When, How?"

Panel: New technology directions for improved VLSI performance

- Prof. Luca Benini, ETH Zurich and University of Bologna
- Mr. Roy Sofer, Satixfy
- Dr. Luca Mattii, Cadence
- Mr. Idan Greenbaum, CEVA

10:45 - 11:30 Coffee break

11:30 - 12:00 Bar-Ilan EnICS and SoC Labs: Status, goals and future

- Prof. Alex Fish, EnICS Labs
- Dr. Adam Teman, EnICS Labs
- Prof. Yossie Shor, EnICS Labs
- Mr. Yonatan Shoshan, SoC Lab

12:00 - 12:45 Lunch

CEVA, Ben-Gurion University and Tel Aviv University: Dynamic Branch Prediction in DSP, From Study to Implementation

- Mr. Udi Sivan, CEVA
- Mr. Kostya Berestizhevsky, TAU

14:00 - 14:25

Dr. Luca Mattii, Cadence
"EDA role In The Design-Technology Co-Optimization Towards N7"

14:25 - 15:15

Mr. Yachin Afek, DSPG
"High performance Class D for portable devices"

15:15 - 15:40

Mr. Dror Goldenberg, Mellanox
"Networking at the Speed of Light"